Q.P. Code: 20EC0448 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Regular Examinations October-2022

DIGITAL ELECTRONICS

(Electrical and Electronics Engineering**)**

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Subtraction by using 1's complement for the given 10101 - 11011.	**L3**	**6M**
	b	Subtraction by using 2's complement for the given 111001-1010.	**L3**	**6M**

OR

2		What is Grey code? What are the rules to construct gray code? Develop the 4 bit gray code for The decimal 0 to 15.	**L1**	**12M**

UNIT-II

3		Minimize the following Boolean function using K-Map F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).	**L2**	**12M**

OR

4		Simplify the following Boolean expressions using K-map. F(A, B, C, D,E)= Σm(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)	**L3**	**12M**

UNIT-III

5		What is Demultiplexer? Desingn1:8 Demultiplexer using 1:4 Demultiplexers.	**L1**	**12M**

OR

6		Design & implement Half Adder and Full Adder with truth table.	**L3**	**12M**

UNIT-IV

7	**a**	Write the differences between combinational and sequential circuits.	**L2**	**6M**
	b	Explain working of Master Slave Flip flop with neat diagram.	**L1**	**6M**

OR

8		Draw the circuit of JK flip flop using NAND gates and explain its operation.	**L3**	**12M**

UNIT-V

9		Explain about Mealy and Moore Models of sequential machines.	**L3**	**12M**

OR

10		What is design procedure for FSM? Give the advantages of FSM.	**L3**	**12M**

*** END ***